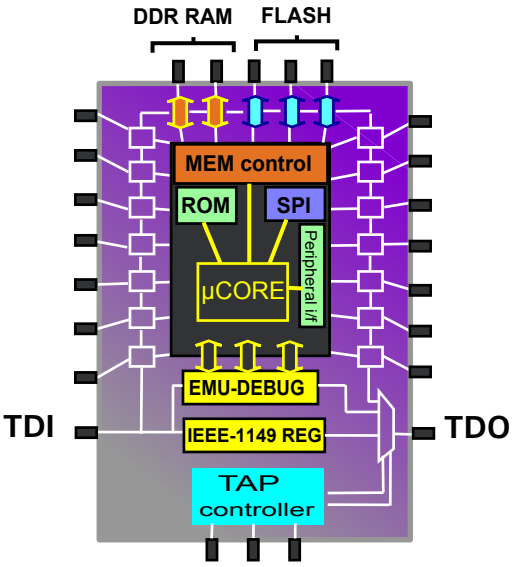
JTAG Technologies CoreCommander Series -

Device Control Via Internal JTAG Access - Processor & FPGA Cores

- Solutions for controlling µProcessors, DSPs & FPGAs from any vendor using debug or ISP access
- Many popular micro cores supported ARM7, ARM9, ARM11, Cortex, XScale, PowerPC, C28x, C166, PIC32 - *not device specific*
- Generic RTL coded solution for FPGAs provides IP core access via Wishbone, Avalon, AMBA etc..
- High level Python™ compatible routines
- Create memory tests, cluster tests and flash programming applications direct from the core
- Overcomes deficiencies in boundary-scan implementation



Block Diagram of CoreCommander Micro interfacing

CoreCommander - *introduction*

Although many devices are now equipped with a JTAG (IEEE Std. 1149.1) boundary-scan register (BSR), a significant number of microprocessors and DSPs can be found with deficient or even non-existent boundary-scan test registers. In the case of today's FPGAs, BSRs have become extended to cover many hundreds of I/O pins and as such are unwieldy, slowing down the test vector rate to an unacceptable level for some tests. For the test engineer this can at best be considered frustrating as he or she looks to employ alternative methods of testing logic cluster elements that may be external to the device or embedded within (e.g. as an IP Core). A new solution however, created by JTAG Technologies, can be used to overcome BSR limitations and in some cases exceed the performance offered by boundary-scan only test access.

Two variants - *designed in-house*

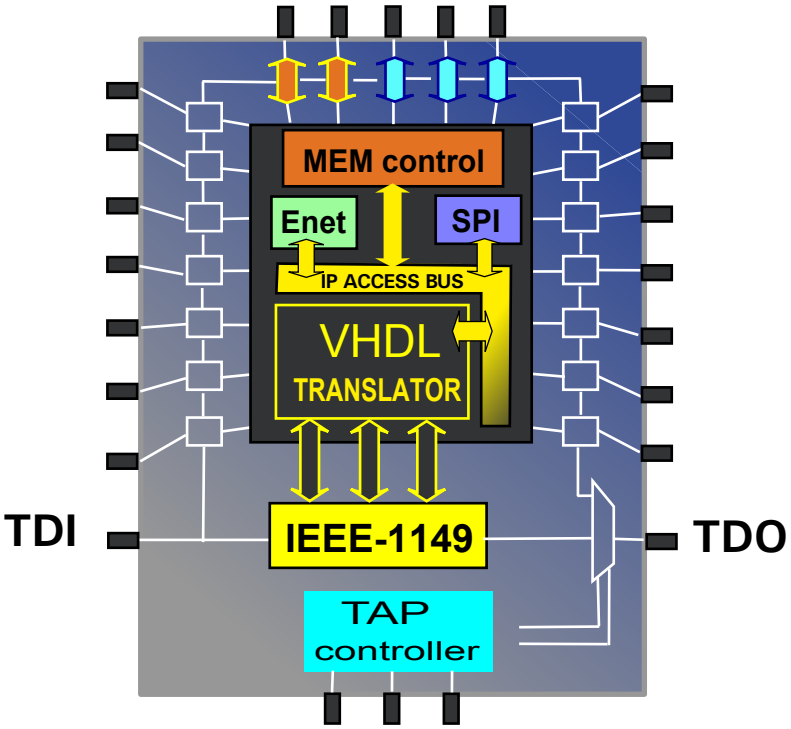
Two allied solutions are offered by JTAG Technologies: CoreCommander Micro takes control of key processor core functions using the built in emulation/debug functions of the processor core, while CoreCommander FPGA uses the bridge features deployed in most FPGAs to access the gate array logic via a generic translator module. The translator in turn provides a conduit to the command and control of IP cores (memory controllers, Bus controllers etc..) via established interface busses such as AMBA, Avalon, CoreConnect and Wishbone.

CoreCommander products are unique in the world of production testing. Designed by test engineers for use by test engineers they are quick to learn and easy to use due to the dual modes of operation, namely 'Interactive' or 'Python managed'

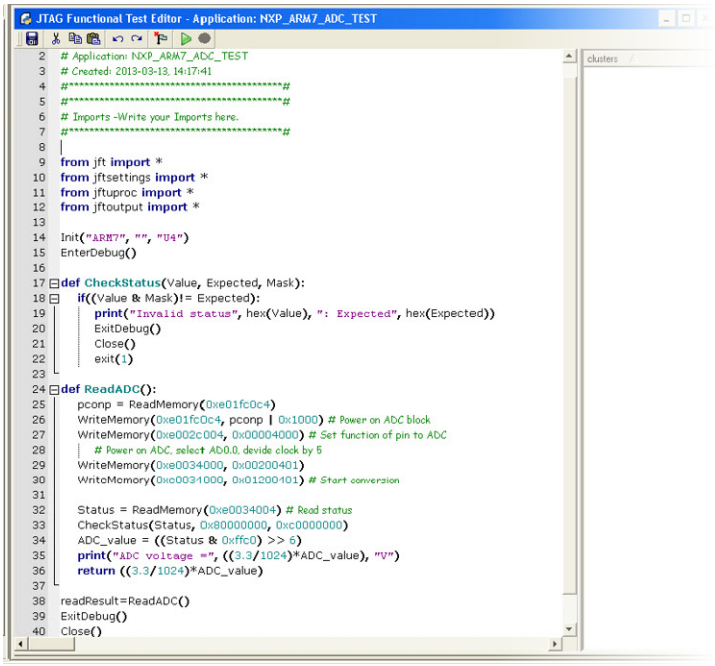
- Interactive mode - allows the user to select a given supported device from within his design and 'manually' select register access commands or full memory reads and memory writes from the interactive window and via a JTAG Technologies controller to the target design. Sequences of commands can be replayed within the interactive window or exported into a Python editor.
- Python-managed mode - using a similar structure to that featured in the JTAG Technologies' JFT (JTAG Functional Test) product, CoreCommander functions can be called from Python code to create re-usable test modules for specific tests. Examples are provided that allow the user to create RAM tests or flash memory programming functions through core operation.

Applications

CoreCommander routines can be used to diagnose 'dead-kernel' boards in design debug since no on-board code is required to set memory reads and writes. BSR deficient parts can also be better harnessed during production test, increasing fault coverage. Hardware engineers can also use CoreCommader FPGA to test the functionality of their chosen IP. Since CoreCommander can be Python-based it complements perfectly the JTAG Technologies JFT products allowing access to analogue parts such as ADCs and DACs and also synchronised testing to full boundary-scan devices.



Block Diagram of CoreCommander FPGA interfacing



Code example using CoreCommander Micro to read an Internal ADC value from an NXP/ARM7 'processor

Summary and ordering details

Prerequisites:-

- Test system requires ProVision JFT or JTAG Live Script for Python embedded usage.

Ordering Information:-

- CoreCommMicro<core>
  <core> = ARM7, ARM9, ARM11, Cortex, XScale, PowerPC, C28x, XC166, Tricore, PIC32

- CoreCommFPGA<vendor>
  <vendor> = Altera, Actel, Lattice, Xilinx

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